

Wide bandwidth frequency modulation of phase lock loops

A new approach to the traditional weakness of frequency modulating a PLL's output.

By David Rosemarin

The phase lock loop is the popular method of frequency synthesis, however one of its main weaknesses is the difficulty in frequency modulating its output. This article will review some of the techniques found in literature, will suggest a new approach and present a practical solution.

The basic PLL

Figure 1 shows a common phase lock loop (PLL) circuit. The loop includes a phase detector, loop filter, voltage controlled oscillator (VCO) and a divider. The sensitivity of the (VCO) is given by:

$$K_0 \text{ (rad/sec/V)} = \Delta\omega/\Delta V = 2\pi\Delta f/\Delta V$$

The sensitivity of the phase detector is:

$$K_p \text{ (V/rad)} = \Delta V/\Delta\theta$$

$F(s)$ is the lowpass filter transfer function.

The PLL can be analyzed by taking the input and output phase as variables.

Since phase is the integral of frequency or $\omega = s\theta$, then K_0/s should be placed as the block for the VCO (see Figure 2.).

The PLL can be, alternatively, be analyzed by taking the input and output angular frequencies as variables (see Figure 3.). A block of $1/s$ should be placed in front of both inputs of the phase detector or the phase detector can be replaced with K_p/s . The transfer function for both block diagrams is actually the same. It is defined by:

$$\theta_o/\theta_i = \omega_o/\omega_i = f_o/f_i = K_p K_0 F(s)/s/D \quad (1)$$

where:

$$D = [1 + K_p K_0 F(s)/s/N] \quad (2)$$

Using a phase modulator

One of the ways often described in literature, to get wideband frequency modulation, is shown in Fig. 4.

Our interest is in understanding the small signal AC behavior of the loop in response to outside stimuli such as modulation. Since the reference frequency is fixed in the FM PLL system, the small signal component of the reference signal is zero. In Figure. 4, two modulating signals are used, V_{m1} and V_{m2} . Using superposition, and knowing that $\omega_0 = s\theta_0$, we get for modulating at V_{m1} :

$$\omega_o/V_{m1} = K_0/D \quad (3)$$

This transfer function has a high pass response and allows frequency modulation of the output frequency at rates greater than the loop bandwidth when a modulation voltage is applied at the V_{m1} input. For modulating at V_{m2} we get:

$$\omega_o/V_{m2} = K_i K_p K_0 F(s)/s/D \quad (3)$$

The transfer function has a nature of a lowpass response and allows for modulating at rates inside the loop bandwidth. If we apply the modulation signal to both the V_{m1} and V_{m2} or $V_{m1} = V_{m2} = V_m$,

then:

$K_m = \omega_o/V_m = K_0[1 + K_i K_p F(s)/s]/D$. And scaling the in-band FM path by setting $K_i = K_0/N$, will obtain a flat frequency response of K_0 . The mathematical result is flat response dependent only on K_0 for modulation rates both inside and outside the loop bandwidth. $F(s)$ block and loop bandwidth do not

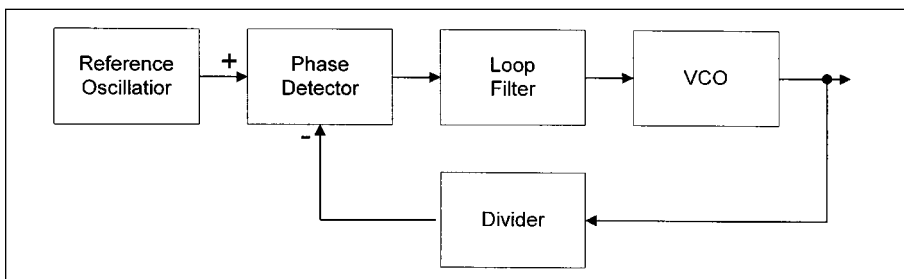


Figure 1. The basic PLL block diagram.

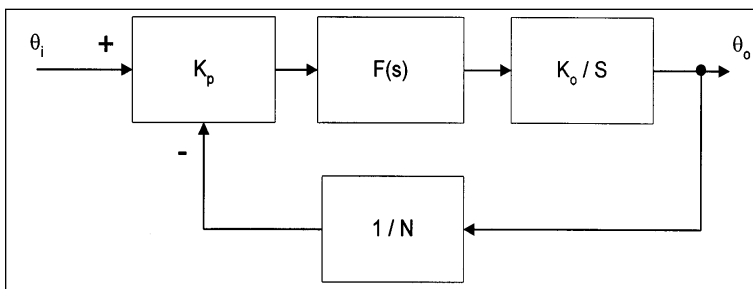


Figure 2. The block diagram using phase variables.

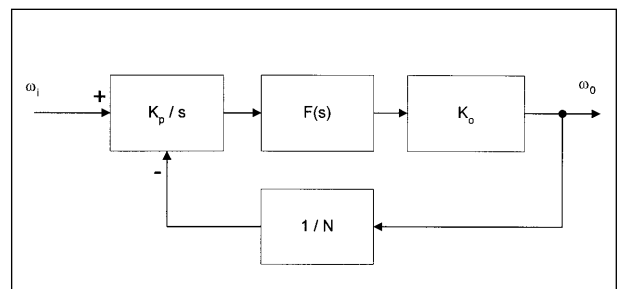


Figure 3. The block diagram using angular frequency variables.

affect the frequency modulation.

There are, however, some limitations to that solution.

(a) Wideband voltage-controlled oscillators have a non-constant K_0 and the PLL has a non-constant divider ratio, N . And, K_i has to vary with output frequency in order to hold a fixed frequency deviation.

(b) A second problem is the integrator. The output of an ideal integrator would slew up and down without bounds when a DC voltage is applied to the input. Any DC offsets at the integrator input will cause a center frequency offset proportional to it. This may be desirable for DC coupled FM, however, for many applications it is necessary to have the output frequency locked at the correct center frequency. In this case, AC coupled FM is needed instead [1].

Modulating the Reference

Figure 5. is a block diagram representing a second approach to modulating. For convenience angular frequency analysis is applied.

Using superposition, and modulating at V_{m1} :

$$\omega_0 = (V_{m1} - \omega_0 K_p F(s)/s/N) K_0, \text{ and } \omega_0/V_{m1} = K_0/D \quad (4)$$

As before, the transfer function has a high pass response and allows frequency modulation of the output frequency at rates greater than the loop bandwidth.

Next, modulating the reference at V_{m2} yields:

$$\omega_0 = (V_{m2} K_R - \omega_0/N) K_p K_0 F(s)/s, \text{ and } \omega_0/V_{m2} = K_R K_p K_0 F(s)/s/D \quad (5)$$

Again, the transfer function has a nature of a low pass response and allows for modulating at rates inside the loop bandwidth. If we apply the modulation signal to both the V_{m1} and V_{m2}

and scaling the in-band FM path by setting $K_R = K_0/N$, we get a flat frequency response of K_0 .

The advantage in this configuration is the elimination of an integrator, but it has, still, some limitations. For example, if a voltage-controlled crystal oscillator (VCXO) has to be used instead of a reference oscillator, there is a limit to its maximum deviation. Also, the maximum modulating frequency into the VCXO has to be much smaller than the parasitic modes of the crystal since there is an overshoot of the audio response at those frequencies.

If the loop frequency is smaller than the frequency of the parasitic modes, a low pass filter can be added at the modulation input of the reference. Its 3 dB frequency should be between those two frequencies so it will not affect at the loop bandwidth but will help in suppressing the incoming signal at frequencies close to the parasitic modes of the crystal.

Modulating in the loop filter

Figure 6 is a diagram of modulation in the loop. Again using superposition and modulating at V_{m1} :

$$\omega_0 = (V_{m1} - \omega_0 K_p F(s)/s/N) K_0 \text{ and } \omega_0/V_{m1} = K_0/D \quad (6)$$

Modulating at V_{m2} yields:

$$\omega_0 = (V_{m2} K_i/s - \omega_0 K_p/s/N) F(s) K_0 \text{ and } \omega_0/V_{m2} = K_i K_0 F(s)/s/D \quad (7)$$

If we apply the modulation signal to both the V_{m1} and V_{m2} and scaling the in-band FM path by setting $K_i = K_p K_0/N$, we get a flat frequency response of K_0 .

As usual there are several limitations of the error corrected FM PLL and reference 2 addresses the particulars.

Because the circuit of Figure 6 blocks part of the loop, it is desirable that a further analysis of the dashed section

of the circuit be analyzed and further simplified. The dashed circuit in Fig. 6 can be re-written as:

$$(V_{m2} K_i/s + V_e) F(s) + V_{m1} = V_0, \text{ and for}$$

$V_{m1} = V_{m2} = V_m$ then:

$$V_m(1 + K_i F(s)/s) + V_e F(s) = V_0 \quad (8)$$

Substituting $K_i = K_p K_0/N$ and using (2) gives us:

$$V_m D + V_e F(s) = V_0 \quad (8')$$

The modified circuit is shown in Fig. 7.

Voltage type Phase Detectors

It would seem that taking an example would be prudent at this time.

A typical lag-lead filter is shown in Figure 8. For reference:

$$F(s) = \frac{1 + s R_2 C_2}{1 + s(R_1 + R_2) C_2} \quad (9)$$

If we try to make a realization of the modulation block " $1 + K_i F(s)/s$ " shown in Figure 7, the process will be performed in the two steps shown in Figures 9a and b. Looking at 9a and using the virtual ground at the inverted input of the operational amplifier and Thevenin's theorem:

$$V_x/V_m = F(s)/2, I = V_x/(2R_1) \\ V_0 = -I/(sC_2) = -F(s)V_m/(s C_a 4R_1)$$

In Figure 9b we added another capacitor and changed the op-amp to a summing amplifier. Therefore:

$$V_0/V_m = -(1 + F(s)/s)/(4 R_1 C_a), \text{ which is equivalent to the first term of (8) or (8'). That assumes that } C_a = 1/(4R_1 K_i) = N/(4R_1 K_p K_0) \quad (10)$$

If a different sensitivity, K_m , is required, Fig. 9b can be modified to 9c and the following relationship can be developed:

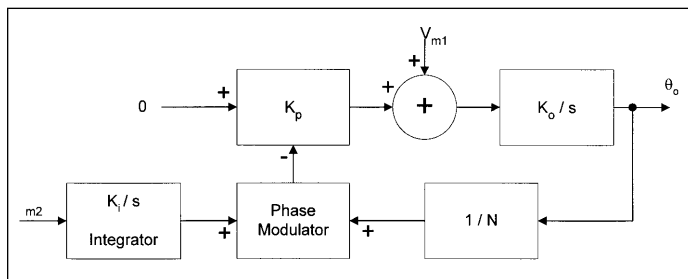


Figure 4. FM using a phase modulator.

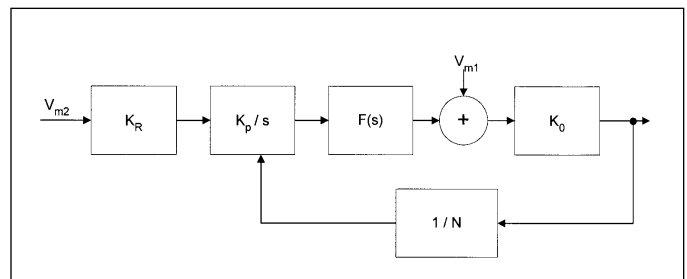


Figure 5. Modulating the reference.

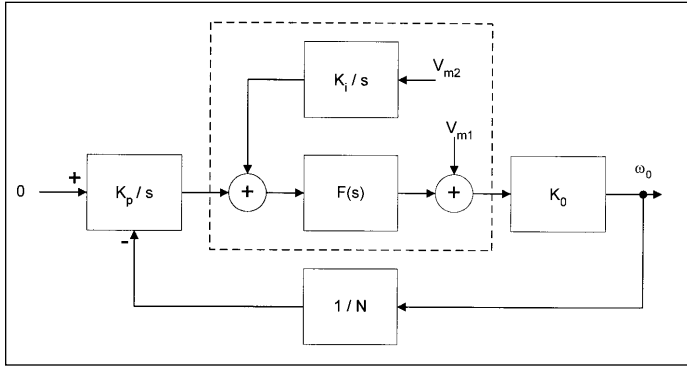


Figure 6. Modulation in the loop.

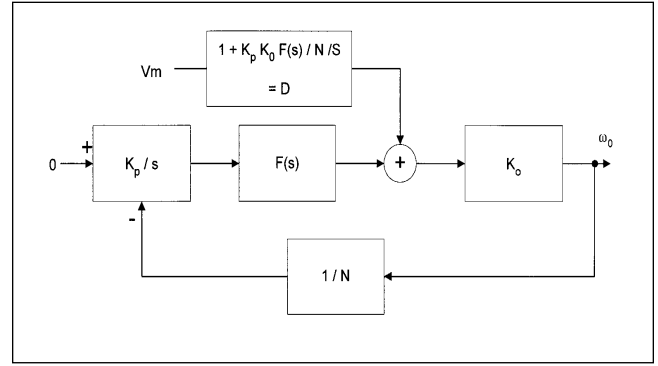


Figure 7. Figure 6 with equivalent circuit.

$$V_o/V_m = -[F(s)/s/(4R_1C_b) + C_a/C_b] = -(C_a/C_b)[1 + F(s)/s/(4R_1C_a)],$$

and:

$$K = -K_0(C_a/C_b)[1 + F(s)/s/(4R_1C_a)]/D.$$

By using Eq. (10), we determine:

$$K_m = K_0C_a/C_b \text{ or } C_b = K_0C_a/K_m \quad (11)$$

This circuit has the limitations of an integrator. Of course, integrator drift can be decreased by limiting the DC gain of the integrator by placing a large value resistor in parallel with C_b . However, this moves the integrator pole of f of zero.

Furthermore, if desired, and with some degradation, the circuit in Figure 9c can be changed into a passive network shown in Figure 10, using the following analysis.

Using Equation (9) and (10) it can be shown that:

$$V_o/V_m = [1 + K_iF(s)/s]/[(C_a + C_b)/C_a + K_i(2 - F(s))/s]$$

and:

$$K_m = K_0C_a/[C_a + C_b + (2 - F(s))/(4sR_1)] \quad (12)$$

From (9), the limits of $F(s)$ are:

$$R_2/(R_1 + R_2) < F(s) < 1, \text{ or } 1 < [2 - F(s)] < 1 + R_1/(R_1 + R_2).$$

The third term in the denominator of (12) can be ignored for all frequencies much greater than f_{\min} where:

$$f_{\min} = 1/(8\pi R_1 C_b) \quad (13)$$

then:

$$K_m = K_0C_a/(C_a + C_b) \quad (14)$$

Obviously, when the ratio K_m/K_0 gets

smaller, C_b has to be larger and f_{\min} is smaller, which means that the frequency bandwidth is larger.

Charge-Pump Phase Detectors

Another technique for phase detector design is using a charge-pump. The following section will derive the design concept for such a circuit. In this case the phase detector sensitivity, K_p , is given by:

$$I/2/\pi \quad (15)$$

A charge-pump loop filter is shown in Figure 11 and the analysis follows.

$V_0 = I_p Z(s)$, and $F(s) = V_0/I_p = Z(s)$. From literature, defining:

$$T_1 = R_2 C_1 C_2 / (C_1 + C_2), \text{ and } T_2 = R_2 C_2 \quad (16)$$

The impedance of Figure 11 was solved by:

$$Z(s) = (1 + sT_2)/(1 + sT_1)/[s(C_1 + C_2)] \quad (17)$$

It has been shown also that:

$$T_1 = (\sec \phi_n - \tan \phi_n)/\omega_n \quad (18)$$

$$T_2 = 1/(\omega_n^2 T_1) \quad (19)$$

$$C_1 = T_1 K_p K_0 \text{ SQRT } \{ [1 + (\omega_n T_2)^2] / [1 + (\omega_n T_1)^2] \} / (T_2 \omega_n^2 N) \quad (20)$$

$$C_2 = C_1 (T_2 / T_1 - 1) \quad (21)$$

$$R_2 = T_2 / C_2 \quad (22)$$

A realization of the modulation block, $D = 1 + K_i F(s)/s$, shown in Figure 7, can be executed by the passive circuit shown in Figure 12. In that circuit, the assumption is made that the resistors, R , are large enough to act as current sources.

Next, determining the following:

$$V_o/V_m = [sC_a + 1/(R^2 N)]/[s(C_a + C_b) + 1/R(1 - 1/(RN))], \text{ where } N = 2/R + 1/Z(s),$$

and assuming that $Z(s) \ll R/2$,

then:

$$N = 1/Z(s) \quad (23)$$

$$V_o/V_m = [sC_a + Z(s)/R^2]/[s(C_a + C_b) + 1/R], \text{ and assuming that } s(C_a + C_b) \gg 1/R \quad (24)$$

$$V_o/V_m = C_a/(C_a + C_b) \times [1 + Z(s)/(sC_a R^2)], \text{ and because } F(s) = Z(s), \text{ equation (2) becomes: } D = [1 + K_p K_0 Z(s)/s/N] \quad (25)$$

$$K_m = K_0 C_a / (C_a + C_b) \times [1 + Z(s)/(sR^2 C_a)] / D \quad (26)$$

and the requirement for K_m to be independent of frequency, is:

$$K_p K_0 / N = 1/(R^2 C_a) \quad (27)$$

then:

$$K_m = K_0 C_a / (C_a + C_b) \quad (28)$$

Additionally, in the above derivation we assumed that $R \gg Z(s)$.

Next, $Z(s_0) = 1/[s(C_1 + C_2)]$, and the requirement for R is:

$$R \gg 1/[2\pi f_{\min}(C_1 + C_2)] \quad (29)$$

Now calculate:

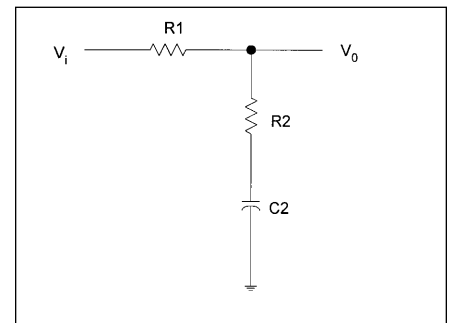


Figure 8. Lead-lag loop filter.

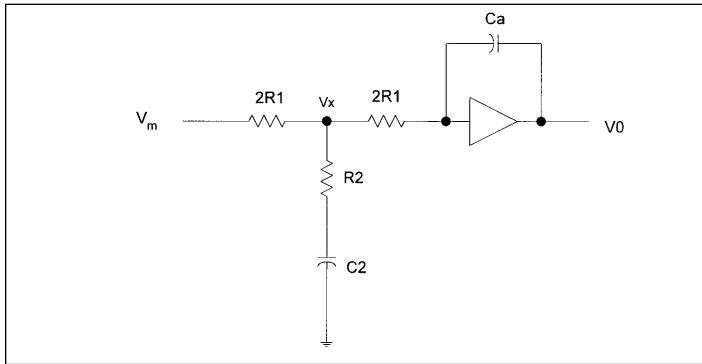


Figure 9a. Realization of $K_v F(s)/s$.

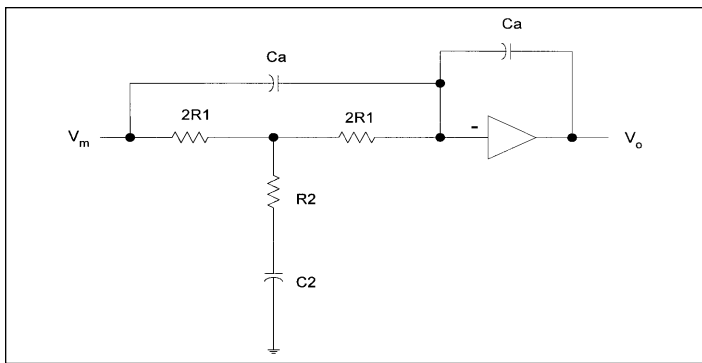


Figure 9b. Realization of $1 + K_v F(s)/s$.

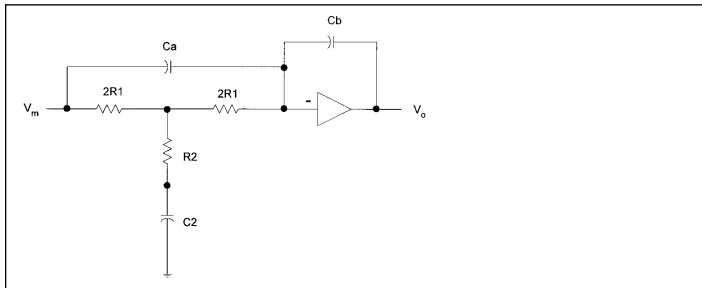


Figure 9c. Changing modulation sensitivity.

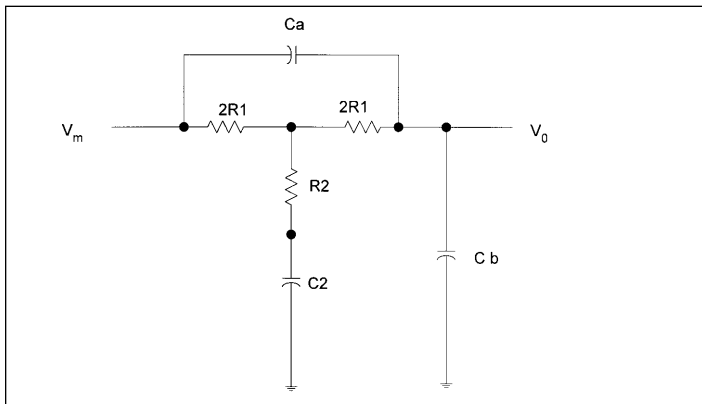


Figure 10. Passive modulator network.

$$R = 20/[2\pi f_{\min}(C_1 + C_2)] \quad (30)$$

then extract C_a from (27), C_b from (28), and build a model for analyzing and optimizing the PLL as described in Reference 7. At this point it is possible to determine a better solution with any standard optimization program.

Element Scaling

If the resistors, R , in the modulation network shown in Fig. 12 are too big, element scaling can be done. Attention should be paid to the fact that the scaling is only in the modulation network and not in the loop filter.

Set the following:

$$\begin{aligned} R_2' &= R_2/m \\ C_1' &= mC_1 \\ C_2' &= mC_2 \end{aligned}$$

Substituting in (16) & (17) leads to:

$$Z'(s) = Z(s)/m$$

Scaling should also be applied to the passive network, which yields:

$$\begin{aligned} R' &= R/m \\ C_a' &= mC_a \\ C_b' &= mC_b \end{aligned}$$

Substituting in (26), with D untouched, leads to $K_m' = K_m$, which means that the modulation sensitivity is invariant with that element scaling. This technique gives us versatility in choosing element values.

Practical configuration

A practical configuration culminates the project by combining both the low-pass loop filter, shown in Figure 8, and the modulation network, shown in Figure 10, is shown in Figure 13. The varicap diode of the VCO is biased by the loop filter at its anode and by the modulation network at its Cathode. This port should have a RF short and a DC return. Sometimes this return is accomplished by the modulation source itself. If not, a large resistor can be connected in parallel to maintain that function.

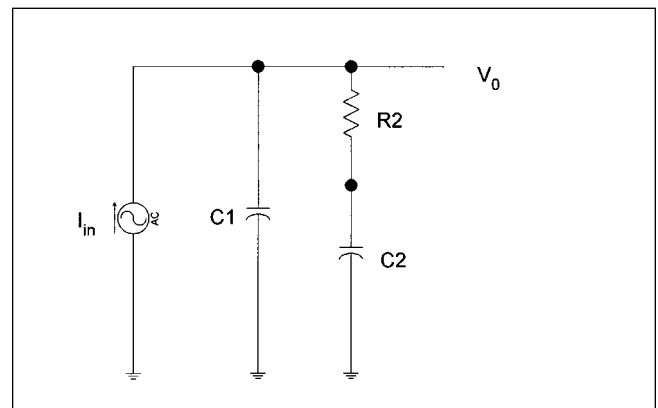


Figure 11. Charge-pump loop filter.

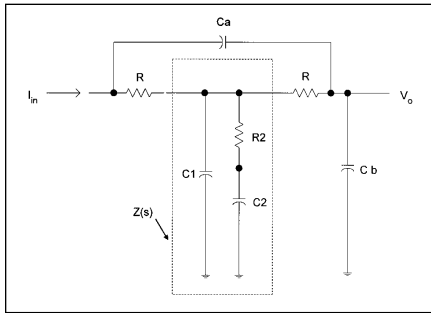


Figure 12. Modulation circuit of the charge-pump PLL.

Conclusion

A very detailed look at the concept of frequency modulating PLL circuits has been presented in this document. It is hoped that this technique will provide the designer with practical tools to assist them in their functionality, and the information is found useful.

RF

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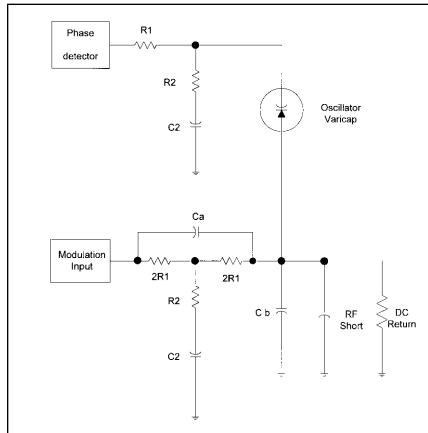


Figure 13. The practical circuit schematic.

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